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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/768,471	01/25/2001	Shinichi Minami	843.39542X00	3956

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EXAMINER	
BAUMEISTER, BRADLEY W	
ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 09/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary

Application No.	Applicant(s)
09/768,471	Minami et al.
Examiner	**Art Unit**
B. William Baumeister	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jul 31, 2003* .

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *4-11, 15-21, 23, and 39-55* is/are pending in the application.

4a) Of the above, claim(s) *4-11, 15-21, and 23* is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *39-55* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☒ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

a. The specification variously sets forth an n-type scattering layer 3 that is formed by implanting phosphorus ions. (See e.g., paragraphs [0057] and [0064] of the substitute specification.) The specification also alternatively refers to well 3 being p-type. (See e.g., paragraph [0061], lines 3 and 8.

Appropriate correction is required.

Claim Objections

2. Claims 43 and 48 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claims 39 and 44, from which claims 43 and 48 respectively depend, sets forth various first and second conductivity type regions. One skilled in the art of semiconductor devices understands that the recitation of first and second conductivity type regions, in and of itself, means that the first conductivity type regions are doped to be either p-type or n-type, and that the second conductivity type regions are doped to be the other of the p-type or n-type. As such, dependent claims 43 and 48, expressly stating this implicitly understood, inherent fact, do not further limit the respective structure of claims 39 and 44.

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 39-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hertrich et al. '533 in view of JP '974 and Howard, Jr. '179.

a. Hertrich discloses an integrated semiconductor structure that includes a plurality of serially connected zener diodes. See e.g., FIG 2 wherein a low-impurity, n-type zone 7 is "applied to" the p-type substrate 6 (col. 3, lines 55-60). A plurality of Zener diodes are formed in the common n- zone 7, each Zener diode comprising a p type semiconductor region 14 (or "second well region") and an n-type ("first") semiconductor region 15. The respective contacts of the diodes are serially connected by metal interconnect 17, which is electrically insulated from the diode by a non-illustrated insulation layer (col. 4, lines 56-).

b. Hertrich does not anticipate the claims for two reasons. First, it does not expressly state whether the "applied low impurity n-type zone 7" is a diffused well (first well region of claim 39), or alternatively is formed by an epitaxially grown method to form an epi-layer as opposed to a well. Second, while teaching serially-connected, lateral Zener diodes, Hertrich does not teach that the Zener diodes may be buried nor possess all of the associated features relating to the specified junction positions and depths and the placement of the contact vias.

c. Regarding the first issue, it was well known to those of ordinary skill in the art at the time of the invention that surface layers/regions of Si semiconductor devices were formed either by epitaxial growth of layers on a substrate or alternatively by the formation of wells within the substrate surface. These two alternative methods of layer formation were functional equivalents: epi-grown layers generally possessed the advantage of higher crystalline quality than diffused wells, and diffused wells possessed the advantage of cheaper manufacturing costs. It would have been obvious to one of ordinary skill in the art at the time of the invention to have formed the "applied n-type zone 7" specifically by a diffusion method--and thereby produce a "first well region"--because this was one of the two conventional ways of forming the functionally equivalent regions and for the purpose of reducing manufacturing costs.

d. Regarding the second issue relating to Hertrich's lacking the teaching that the serially-connected Zener diodes may specifically be of the buried-Zener diode type, JP '974 (previously made of record) discloses a buried Zener diode structure comprising an n-type (type I) semiconductor region 1; a p-type well region (type II second well region) 2; a first, n-type semiconductor region 10 formed in the second well 2; a second, p-type semiconductor region 9 formed in the well 2 at the bottom of only the central portion of n-region 10. The p-region 9 is more heavily doped (1e16) than the p-type well 2 (5e15) (page 3, lower right column) (e.g., claims 24, 26 and 27). A plurality of through holes extend through insulating layer(s) 3 and/or 13, and comprise a plurality of first connection holes 6 (extending from wiring layer 8) for providing electrical connections therethrough to said first n-type semiconductor region 10; and a plurality of

second connection holes 6 (extending from wiring layer 7) for providing electrical connections therethrough to said second, p-type well region 2 (by way of p+ contact region 5). Semiconductor regions 9 and 10 form a first pn junction. N-type substrate/region 1 and p-well 2 form a second pn junction. As the Zener breakdown occurs between the first pn junction, producing a current Iz (FIG 2), the breakdown voltage of the second pn junction is greater than that of the first junction.

e. It would have been obvious to one of ordinary skill in the art at the time of the invention to have provided buried Zener diodes as taught by JP '974 for the serially-connected Zener diodes of the Hertrich '533 circuit for the purpose of obtaining the benefits previously known to be associated with the buried pn-junction Zener diode structure. These known benefits include reducing/preventing interface leakage currents (see e.g., the present application's substitute specification, BACKGROUND OF THE INVENTION section, paragraph [0003]); and preventing the negative influence of the depletion region, and providing decreased operation resistance, as taught by JP '376, English Abstract, cited hereinbelow in the Conclusion section.

f. To summarize, the combination of Hertrich/JP '974 teaches the use of buried Zener diodes in circuits that include a plurality of serially-connected Zener diodes that are formed in an n-region that, in turn, overlies a p-type substrate. JP' 974 further teaches that the wiring 8 is connected to the n+ type semiconductor region 10 by means of a plurality of spaced-apart vias 6 that are disposed over the entire surface of the semiconductor region 10, which increases the evenness of the current distribution therebetween. The combination of Hertrich/JP '974, alone,

does not render these claims obvious because JP '974 does not teach the further inclusion of the first (n type) semiconductor region 10 possessing a peripheral portion forming a deeper junction depth with the second well region 2 than does the central portion. As such, JP '974 also does not further teach the vias 6 being formed over such a deeper-junction peripheral portion of the region.

g. Howard '179 (previously made of record) teaches buried Zener diode structures comprising a p-region 24 and an overlying n-region 32 forming the pn junction are formed in N well 16 on p substrate 10. The metalization pattern extend through the overlying insulation to contact a portion of the n region (C) at a peripheral region remote from the shallowest portion of n-cathode 32 for the purpose of preventing spikethrough or shorting problems (col. 5, lines 40-). It would have been obvious to one of ordinary skill in the art at the time of the invention to have further provided the n-type cathode layer 10 of the JP '974 buried Zener diode structure with a deeper-junction peripheral portion with the disclosed vias instead contacting this peripheral portion for the purpose of preventing spikethrough as taught by Howard. It would have been further obvious to the skilled artisan to have provided the plurality of vias so as to surround the region's periphery--instead of Howard's teaching of providing a single via only at one side of the region--for the purpose of more evenly distributing the current as taught by JP '974.

h. Regarding claim 54, regardless of whether any of these references teaches that the conductivity types may be reversed, it was well known to those of ordinary skill in the art at the time of the invention to reverse the conductivity types of all of the regions within a semiconductor

structure depending merely upon the particular larger circuit in which the structure is specifically to be formed.

Response to Arguments

5. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Prentice et al. '664 teaches lateral-contact, buried junction Zener diodes (see e.g., FIG 12).

b. JP '533 teaches lateral-contact, buried junction Zener diodes (e.g., FIG 1) and teaches that the buried-junction structure is not affected by the depletion layer, and provides decreased operation resistance. (English Abstract)

INFORMATION ON HOW TO CONTACT THE USPTO

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to the examiner, **B. William Baumeister,** at **(703) 306-9165.** The examiner can normally be reached Monday through Friday, 8:30 a.m. to 5:00 p.m. If the Examiner is not available, the Examiner's supervisor, Mr. Eddie Lee, can be reached at (703) 308-1690. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

B. WILLIAM BAUMEISTER
PRIMARY EXAMINER

B. William Baumeister

Primary Examiner, Art Unit 2815

August 31, 2003